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# Improving Yield and Performance in ZnO Thin-Film Transistors Made Using Selective Area Deposition

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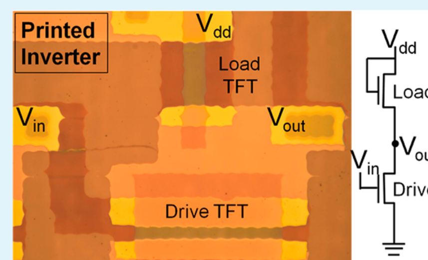
**ABSTRACT:** We describe improvements in both yield and performance for thin-film transistors (TFTs) fabricated by spatial atomic layer deposition (SALD). These improvements are shown to be critical in forming high-quality devices using selective area deposition (SAD) as the patterning method. Selective area deposition occurs when the precursors for the deposition are prevented from reacting with some areas of the substrate surface. Controlling individual layer quality and the interfaces between layers is essential for obtaining good-quality thin-film transistors and capacitors. The integrity of the gate insulator layer is particularly critical, and we describe a method for forming a multilayer dielectric using an oxygen plasma treatment between layers that improves crossover yield. We also describe a method to achieve improved mobility at the important interface between the semiconductor and the gate insulator by, conversely, avoiding oxygen plasma treatment. Integration of the best designs results in wide design flexibility, transistors with mobility above 15 $cm^2/(V\ s)$, and good yield of circuits.




**KEYWORDS:** *thin-film transistor, metal oxide, zinc oxide, selective area deposition, atomic layer deposition, spatial ALD, TFT yield*

## ■ INTRODUCTION

In the early stages of an emerging technology, research activity is typically focused on demonstrating feasibility of ideas and concepts. For example, until recently, publications on printed electronics tended to report on the performance of novel materials and novel fabrication techniques, while issues of yield, reliability, and stability went largely unaddressed. Ultimately, however, all materials systems and processes have inherent limitations and defects that must be identified and mitigated in order to further progress a technology toward a commercial reality. Recent work in the printed electronics field has turned to investigating the real issues with defined materials sets and process tools,[1,2] and demonstrating creative approaches to practical circuitry.[3]

The phrase "printed electronics" covers a wide array of approaches. In our approach, thin-film metal oxide devices are formed using selective area deposition (SAD), by using an inkjet-printed inhibitor to pattern inorganic films grown by spatial atomic layer deposition (SALD).[4] In atomic layer deposition (ALD), deposition of an atomic layer is the outcome of a chemical reaction between a reactive molecular precursor and the substrate. ALD is thus inherently a very surface-sensitive deposition technique, and selectively inhibiting growth by ALD on a substrate has been explored by a number of groups.[5−8] As the name implies, SAD involves treating portions of a substrate such that a material is deposited only in those areas that are desired, or selected.

Types of functional materials that can be deposited with ALD include conductors, dielectrics or insulators, and semiconductors. ALD can thus be used as a fabrication step for forming thin-film circuits, including thin-film transistors (TFTs) and supporting electronic components such as resistors, capacitors, insulators, and bus lines. In capacitors and TFTs, defects in the insulating layer can allow short-circuits between conductive elements that can be catastrophic for individual devices as well as the circuits containing them. Approaches to forming high-quality dielectric layers typically fall into one of two categories: a single thick layer of a single material or multiple layers of different material types.[9−11] In the case of bottom gate devices that use a single-layer dielectric, large thicknesses (>100 nm) are often used to ensure high device yield.[9] In general, however, thick dielectrics are undesirable because of the longer deposition times, and furthermore the resulting devices require a higher operating voltage.

In both approaches to high-quality dielectric formation, process and environmental conditions are also controlled to reduce the likelihood of defect formation. For example, the expensive and strict clean-room environments used in traditional semiconductor fabrication facilities are necessary to achieve good yield in complementary metal oxide semiconductor (CMOS) circuitry. For printed electronics, however, the drive is toward materials and methods with lower cost, and which can be used on a variety of substrates to build distributed functionality rather than the high density of features in typical CMOS wafers. The desired manufacturing environment for printed electronics looks more like a print-house or a roll-to-roll manufacturing facility rather than the clean-rooms associated with Si processing. One of the challenges in printed electronics is managing the defect density for the associated large feature

Received: November 10, 2014
Accepted: January 6, 2015
Published: January 6, 2015

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DOI: 10.1021/am5077638
ACS Appl. Mater. Interfaces 2015, 7, 2754−2759

sizes in this less controlled environment. This can be addressed in many ways, from redundant circuit design to robust materials, and to robust processes. We perform our research in standard chemistry laboratories, which include chemical fume hoods and unfiltered air, for both convenience and as a proxy for the less-than-ideal conditions of the envisioned printed electronics manufacturing environment.

We have previously explored the temperature and exposure-time phase space for SAD with our most common SALD precursors using polyvinylpyrrolidone (PVP) as the inhibitor material.[12] We have also demonstrated using patterned-by-printing methods to build full thin-film transistors with aluminum-doped zinc oxide (AZO) conductors, nitrogen-doped zinc oxide (ZnO:N) as the semiconductor, and aluminum oxide ($Al_2O_3$) as the insulator.[4] This patterned-by-printing approach uses dimethylaluminum isopropoxide (DMAI), a less reactive precursor than trimethylaluminum (TMA), for the $Al_2O_3$ insulator, to enable the use of SAD. The patterned-by-printing process involves first printing an inhibitor in the inverse of the desired functional pattern, followed by the growth of the desired thin film using SALD. After SALD growth, the inhibitor is removed, typically by using an oxygen plasma. The result of this process step is that each layer is grown on a surface that has been subjected recently to an oxygen plasma, and each functional layer has a surface that is subjected to a plasma treatment.

In this paper, we describe systematic approaches to improvement in both performance and yield for electronic devices patterned by printing. We have explored methods to decrease shorting defects in the insulator, as defects in the dielectric layer are most critical for the yield of capacitors, transistors, and circuits. In addition, as the interface between insulator and semiconductor is critical to transistor performance, we also explored methods to control and improve the insulator/semiconductor interface in patterned-by-printing transistors.

## ■ EXPERIMENTAL SECTION

**SALD Depositions.** Clean borosilicate glass served as the substrate for all experiments. As described in more detail in previous publications,[4,12,13] the precursors for ZnO:N are diethylzinc (DEZ) and water vapor mixed with ammonia gas, whereas for $Al_2O_3$ the precursors are water and either TMA or DMAI, and depositions are performed at 200 °C. All SALD depositions were done using a 50 ms residence time (for both of the precursors and for the inert nitrogen purge) by controlling the velocity of the substrate over the SALD head. At 200 °C, ZnO from DEZ and alumina grown from TMA are in the saturated portion of the ALD growth curve, which is to say additional exposure to reactants does not produce further reactions on the surface. In contrast, alumina grown from DMAI is in the unsaturated portion of the ALD growth curve, meaning that there is insufficient exposure to the precursors within a cycle to fully form a monolayer of growth.

**Film Characterization.** Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was performed in the positive polarity mode with $Bi^{3+}$ cluster analysis and 3 kV Ar sputter beam. Atomic Force Microscopy (AFM) scans for roughness analysis were performed in tapping mode over 10 $\mu$m image areas. Two scans from different regions were averaged for each sample. X-ray diffraction (XRD) measurements were taken over a $2\theta$ range of 0−40°.

**Fabricating TFTs with Photolithography.** The TFTs arrays for yield-testing were fabricated with patterned Cr gates that were oxygen plasma cleaned immediately before uniformly depositing an $Al_2O_3$ dielectric layer using SALD. After each dielectric layer was deposited, the substrate was removed from the SALD head, thereby exposing the dielectric surface to room atmosphere before the substrate was replaced on the SALD head for the blanket ZnO:N deposition. After ZnO:N deposition, the substrates were coated with PMMA and Microposit S1813 photoresist for double-layer lithography, in which the source/drain pattern was exposed and developed in the S1813, and an oxygen plasma was used to etch through the revealed underlying PMMA. Substrates were then water-rinsed, blown dry, and 70 nm of aluminum metal was deposited using an evaporator. Lift-off was performed in acetone, with an IPA rinse. Isolation of the individual TFTs was achieved by patterning with PMMA and etching the exposed ZnO layer with a dilute acetic acid solution. The PMMA layer was left in place, as can be seen in the inset of Figure 2. Channel width was 200 $\mu$m, length was 30 $\mu$m, and the gate overlap area of the device is close to 300 × 300 $\mu$m. We used an array of 400 nominally identical TFTs as the means to test yield over the area 1.2 × 3.8 cm of deposition on each glass substrate.

**Patterned-by-Printing TFT Fabrication.** Prior to each printing step, the substrate was cleaned with a 2 min (0.3 Torr 100 W) oxygen plasma, which gives a reproducible growth surface. We used a Fuji Dimatix 2500 printer with a 10 pL print head to inkjet a PVP-based inhibitor ink in an inverse pattern of each functional layer desired.[4] A schematic of this is shown in Figure 1a. The SALD system then

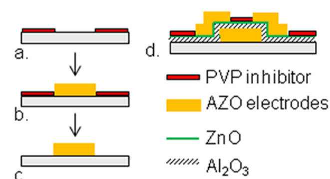


**Figure 1.** Schematic process flow for printed TFTs. (a) Inhibitor printed where no growth is desired. (b) Inorganic layer, in this case the AZO gate, deposited by SALD. (c) Inihibitor pattern removed using oxygen plasma, leaving the substrate ready for the next inhibitor pattern. (d) Completed bottom-gate, staggered-contact TFT, with inhibitor which selectively patterned the source/drain electrodes still in place.

deposited a functional layer in the spaces where there was no inhibitor, as illustrated in Figure 1b. The gate electrode was a selectively deposited 100 nm thick layer of AZO with a contact pad at one end. The inhibitor pattern for the gate was then removed using an oxygen plasma, leaving the substrate and gate layer ready for the inhibitor pattern for the dielectric, as shown in Figure 1c. The DMAI-based dielectric layer was patterned with PVP inhibitor ink protecting the gate contact pad, so no dielectric grows there, forming a "via". For substrates with a two-layer primary dielectric, after deposition and plasma cleaning of the first layer of $Al_2O_3$, the same pattern was reprinted to selectively inhibit the growth of the second layer. The buffer/semiconductor pattern was a small rectangular opening centered on, and crossing, the gate. Finally, as illustrated in Figure 1d, 100 nm thick AZO source and drain electrodes were formed to overlap the gate and semiconductor patch, with the channel gap defined by a single printed row of inhibitor ink drops, defining the channel length of 90 $\mu$m, whereas the channel width is defined by the 400 $\mu$m wide semiconductor.

**Electrical Testing.** Electrical testing of TFTs was performed using an automated probe station and an Agilent 4155C parameter analyzer. For each substrate, the gate voltage was scaled to give an equivalent electric field for the given dielectric thickness to stress the devices in a comparable way when measuring the transfer characteristics. Field-effect mobility is extracted from linear transfer characteristics, taken at drain voltage of 0.2 V, using the standard gradual channel approximation.[14] In calculating yield, a "good" device was defined as a functional TFT ($V_{th} > 0$, mobility > 1) with gate leakage current below $1 \times 10^{-7}$ A at the maximum applied gate voltage (where the typical gate leakage is $\leq 10^{-10}$ A.) The ring oscillators were driven using an Agilent 6613C 0−50 V power supply, and the response was recorded using a Tektronics TDS 2024B oscilloscope.


DOI: 10.1021/am5077638
ACS Appl. Mater. Interfaces 2015, 7, 2754−2759

## RESULTS AND DISCUSSION

**Improving the Gate Insulator.** We first focused on defects inherent in the as-deposited materials by using traditional photolithography rather than SAD to fabricate devices. We can thus avoid convolving the yield from material properties with yield issues associated with ink jet printing.

As a baseline, substrates with arrays of TFTs with TMA-based $Al_2O_3$ were fabricated over a range of dielectric layer thicknesses. $Al_2O_3$ grown by ALD from TMA and water is a well-studied, high-quality dielectric material.[15] A comparison of the yield as a function of dielectric thickness can be seen in Figure 2. The substrates with TMA-based $Al_2O_3$ dielectric,

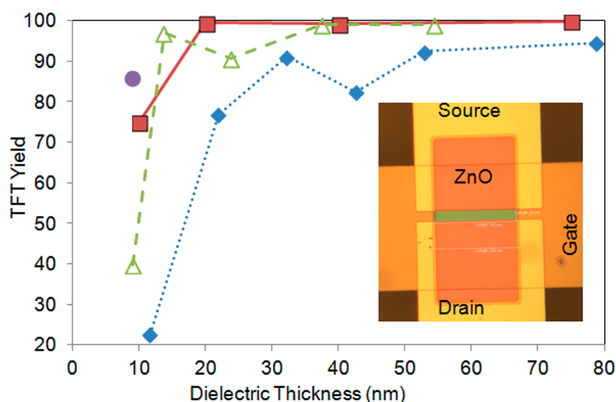


**Figure 2.** Percent yield for ZnO-based TFTs with different growth processes and varying $Al_2O_3$ gate insulator thickness. Each point corresponds to one substrate. A total of 395 devices were characterized on each substrate, and devices with gate leakage above $1 \times 10^{-7}$ A were considered to have failed. The squares correspond to samples with a single layer of TMA-based $Al_2O_3$, diamonds to single-layer DMAI-based $Al_2O_3$, triangles to double-layer DMAI-based $Al_2O_3$, and the circle to a triple-layer DMAI-based $Al_2O_3$. The inset shows an example device with Cr gate, blanket dielectric, isolated ZnO semiconductor, and aluminum source and drain electrodes, with $W/L = 200\ \mu m/30\ \mu m$.

shown by filled squares, have >99% yield over the range from 20 to 75 nm, dropping to 75% yield at 10 nm. Using a simple calculation that counts a failed TFT as a single insulator-shorting defect, and knowing the overlap area in each device, we find that the use of the highly reactive TMA precursor, despite noncleanroom processing, results in defect rates of fewer than $10/cm^2$ for layer thickness as low as 20 nm.

In contrast, the device yield from substrates with a single dielectric layer grown using the DMAI precursor, shown in Figure 2 by diamonds, nearly saturates at close to 90%; the maximum yield was 94% at the thickness of 78 nm, corresponding to over 60 defects/$cm^2$. (The yield in the device with 42 nm dielectric was anomalously low, and suffered from photolithography issues.) This curve suggests that manufacturing circuits with a single DMAI-based dielectric layer is not a promising path, because there is a high possibility of failure in the insulator of both TFTs and crossovers, even when using a relatively thick dielectric layer. Thus, circuits, which both cover a relatively large substrate area, and require multiple devices each to work in order to function, become particularly difficult to produce successfully.

In a second series of substrates with DMAI-based alumina dielectric layers, we split the dielectric into two layers, each with a separate growth event. After the first layer was grown to half the total desired thickness, the substrate was removed from the SALD head and exposed to an oxygen plasma for 2 min, as would be typical in our patterned-by-printing technique. After plasma treatment, the second half of the dielectric layer was grown using the same conditions as the first layer, and the sample was completed as above. The yields of substrates grown with two-layer DMAI-based dielectric are shown by open triangles in Figure 2. Even at a thickness of 14 nm, the yield (97%) is better than that of the thickest single-layer DMAI-based substrate shown. The potential to yet further improve the yield is indicated by a solid circle at the thinnest dielectric (9 nm), where building the thickness by three layers gives a yield of 86%, compared to the yield of 52% for a double layer.

Our hypothesis for this improvement is that defects in the first layer of the dielectric are prevented from propagating through the second layer of the dielectric by the plasma treatment. We know that unintentional surface contamination can act locally as an inhibition agent for DMAI growth, and thus could cause pinholes or shorting sites in the dielectric layer. ALD growth using DMAI is sensitive to surface chemistry, and is therefore amenable to SAD, but can be negatively impacted by surface contaminants. An oxygen plasma can either remove contamination acting as an inhibiting agent, or change its surface properties so that it is no longer inhibiting, effectively allowing growth at that region. Presumably, additional unintentional contaminants populate the newly cleaned surface, randomly located with respect to the first set of defects. Thus, the position of defects is uncorrelated and the dielectric is electrically more robust.

To address the question of whether DMAI-grown $Al_2O_3$ grows differently on the plasma-cleaned surface, we grew a series of samples with thick $Al_2O_3$ films built up by different numbers of growth events separated by exposure to oxygen plasma. X-ray diffraction (XRD) shows no discernible difference between an $Al_2O_3$ film grown in a single layer (75 nm thick) and films grown in 4, 6, or even 10 layers (100 nm total thickness). Every sample was amorphous.

The samples, however, are not equivalent in either their surface properties or their internal composition. The internal interfaces formed between layers can be detected chemically by SIMS. As seen in Figure 3, a single layer shows a smooth signal for the aluminum hydroxide (AlOH) peak, whereas a four-layer multilayer has peaks at the expected interface locations.

The surface roughness of the single thick $Al_2O_3$ layer is also different from the surface roughness of $Al_2O_3$ deposited in multiple growth steps separated by oxygen plasma exposure. Root-mean-square roughness measurements are the average taken over two 10 $\mu$m scans from different areas. As shown in Table 1, the smoothest surface results from the extreme case of a 100 nm thick layer grown in 10 nm steps, each with an oxygen plasma prior to growth, where the RMS roughness was 0.21 nm. In comparison, a single 75 nm thick layer had RMS roughness of 0.40 nm. Additional multilayer samples were grown with unequal increments, as described in Table 1. In each case, the samples were removed from the deposition head between layers and thus exposed to room atmosphere, while samples in the right-hand column were also exposed to a 2 min oxygen plasma. The bottom two rows in the table illustrate that the order of growth of different thickness layers is much less important than whether there was or was not a plasma treatment between growth steps, with a clear signal that plasma treatment decreases surface roughness. The decreased roughness for plasma-treated layers relative to the same structure


DOI: 10.1021/am5077638
ACS Appl. Mater. Interfaces 2015, 7, 2754–2759

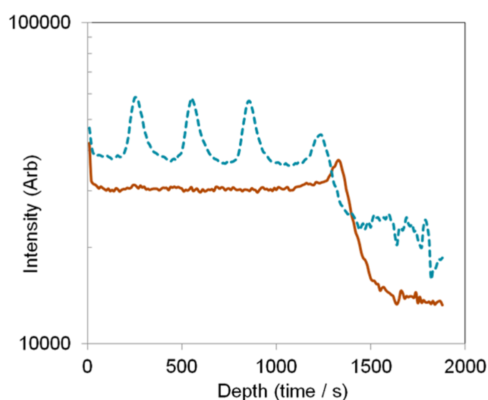


**Figure 3.** AlOH signal from SIMS analysis of single- and multilayer DMAI-based $Al_2O_3$. Solid line corresponds to 80 nm thick single layer, whereas the dashed line corresponds to a layer of similar thickness built up by four layers, each 20 nm thick, with an oxygen-plasma step between them.

**Table 1. Root-Mean-Square Roughness of DMAI-Grown $Al_2O_3$ Grown with Different Stacks**

| layer structure | no plasma | plasma |
|---|---|---|
| 75 nm | 0.4 ± 0.01 | |
| 10 nm × 10 | | 0.21 ± 0.00 |
| (25 nm × 2) + (10 nm × 5) | 0.59 ± 0.01 | 0.25 ± 0.02 |
| (10 nm × 5) + (25 nm × 2) | 0.57 ± 0.02 | 0.3 ± 0.01 |

without plasma suggests, as does the reduction in defects, a resetting of the growth surface to one with a relatively uniform probability of growth.

The room-temperature transistor performance is evidently not sensitive to this, as we see no difference in average hysteresis nor change in mobility for a given final thickness of $Al_2O_3$, whether grown in one or in multiple steps. For the substrates evaluated for DMAI-based $Al_2O_3$ yield above, using a dielectric constant value of 7, the average mobility with thicker dielectric were all about 17 $cm^2/(V\ s)$. The calculated mobility drops for dielectric layers thinner than 15 nm. However, according to reports in the literature, the dielectric constant drops for thinner layers of alumina,[15] which would account for the apparent mobility drop.

**Improving the Dielectric/Semiconductor Interface.** Field-effect mobility of a transistor depends not only on the bulk mobility of charges in the semiconductor but also depends critically upon the interface between the dielectric and the semiconductor. This is the interface at which charge accumulates, thus details of the bonds between semiconductor and insulator, as well physical roughness and chemical inhomogeneity, can dramatically affect the transport. Even at room temperature, the mobility extracted from a TFT can be a sensitive metric for the quality of the interface.

In the method we have developed for patterning-by-printing TFTs, the inhibitor pattern must be changed between the dielectric and the semiconductor to prevent shorting to the gate at edges of the pattern. Typically, the dielectric layer is formed over the entire substrate, with vias where necessary to connect layers of conductor or to allow access for electrical testing. The semiconductor pattern is used to isolate the individual transistors and is chosen so that material only deposits locally. The insulator surface is thus exposed to an oxygen-plasma step to remove the insulator "via" pattern prior to being printed with the semiconductor inhibitor pattern. In general, TFTs patterned with this process show noticeably lower mobility than those processed with photolithography (and thus without the need for the plasma step, as all patterning takes place after deposition.)

To probe this decrease in mobility, and to potentially improve the dielectric/semiconductor interface, we explored the effect of growing a thin buffer layer of $Al_2O_3$, after what we will now designate as the "primary" dielectric layer, and just before we grow the ZnO:N layer. The series of samples had the same design as the yield-test substrates, with a two-layer 50 nm thick DMAI-based primary dielectric that was exposed to a 2 min oxygen plasma after deposition. ZnO:N was either grown on the dielectric surface immediately after plasma, or an additional specified thickness of $Al_2O_3$ buffer layer was grown, followed by the ZnO:N layer. In both cases, the substrate was removed from the deposition head and exposed to room conditions between insulator and semiconductor. The devices were then completed as described above. The resulting mobility (averaged over 250 devices) is plotted in Figure 4 as a function of the buffer layer thickness.

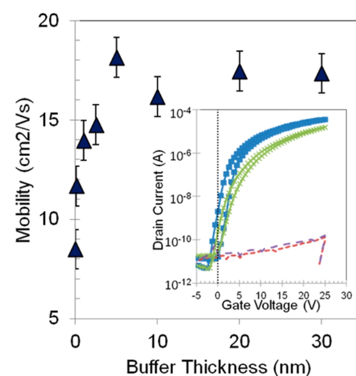


**Figure 4.** Effect of $Al_2O_3$ buffer layer on average TFT mobility, averaged over 250 devices per substrate. The dielectric thickness for each substrate was 50 nm of primary dielectric, plus the buffer layer thickness. Inset: linear region transfer curve ($V_d$ = 0.2 V) for TFT with no buffer layer (green crosses), compared to 5 nm buffer layer case (blue squares). Gate leakage, shown in dashed lines, is similar for the two samples.

The lowest mobility sample, at 8 $cm^2/(V\ s)$, was the one with no buffer layer (consistent with the mobility we reported for the patterned-by-printing "no buffer layer" TFTs in ref 4.) Even a nominal 0.1 nm buffer layer improves the average mobility to about 12 $cm^2/(V\ s)$, whereas the anticipated mobility of about 17 $cm^2/(V\ s)$ (as achieved in the first experiment above) is reached with a buffer layer of 5 nm. Example linear region transfer curves are shown in the inset of Figure 4 for a TFT with a 5 nm buffer and one without a buffer. The subthreshold slope for TFTs without a buffer was worse than those with a buffer, as is expected from more interface states between insulator and semiconductor.

**Printing TFTs.** Although we used lithographically patterned TFTs to explore the device improvements above, these improvements are most applicable to patterned-by-printing devices. In photolithographically defined devices, using highly reactive TMA as the precursor for $A_2O_3$, and keeping the interface between the dielectric and semiconductor free of processing, is straightforward. However, in the patterned-by-printing process, DMAI is the preferred precursor for the


DOI: 10.1021/am5077638
ACS Appl. Mater. Interfaces 2015, 7, 2754−2759

$Al_2O_3$, because the TMA precursor is so reactive it is difficult to inhibit its growth.[16] The dielectric layer is therefore more prone to defects, requiring the multilayer process for better yield. Furthermore, the inhibitor pattern needs to be changed between the primary insulator and semiconductor, thus requiring a buffer layer for higher mobility.

For the experiments described above, a blanket layer of both the buffer dielectric and the semiconductor were deposited and then patterned. To achieve the same control of the interface using SAD, we must selectively allow the growth of both the dielectric and the semiconductor with the same printed inhibitor pattern. Interestingly, because the same inhibitor ink is effective for all the deposited materials, multiple layers of different materials can be patterned without changing the inhibitor. The printed inhibitor is effective until there is nucleation of growth on the inhibitor surface, and in this case it is critical that the first material ($Al_2O_3$) has not nucleated on the inhibitor before starting deposition of the second material (ZnO). Given the relatively thin buffer and semiconductor layers, we are well within the selective growth regime and thus can use one pattern to form the buffer layer and ZnO layer in our patterned-by-printing approach. We have successfully grown $Al_2O_3$ buffer layers over a thickness range from 2.5 to 30 nm, with a ZnO:N semiconductor layer on top with a thickness ranging from 10 to 60 nm, using a single printed PVP pattern.

An experiment with five substrates was designed to independently probe the impact of the multiple layers of dielectric, the buffer layer pattern, and the use of oxygen plasma at the interface between the dielectric and the semiconductor. All of the samples were designed to have 75 nm of gate dielectric under the channel. The channel width was defined by the semiconductor, while source/drain electrodes extended over a larger region of the gate. This geometry is preferred in some cases because the current is strictly confined and an accurate calculation of mobility can be made using the width and length. However, it also means that the yield of the device depends most strongly upon the quality of the primary $Al_2O_3$ dielectric layer, rather than the full stack with buffer and semiconductor.[17]

As a baseline control, substrate A was prepared with a primary (and only) dielectric made in a single layer and with a 2 min oxygen plasma clean prior to printing the pattern for the semiconductor. Substrates B and C had a single primary dielectric layer of 50 nm, whereas substrates D and E had a two-layer primary dielectric formed from 25 nm layers with a plasma treatment between them. For B, C, D, and E, after the primary dielectric was deposited and the inhibitor plasma-cleaned, a 25 nm additional layer of $Al_2O_3$ was grown with the same pattern as the semiconductor. Oxygen plasma was used to remove the inhibitor pattern on substrates B and D after the additional $Al_2O_3$ was grown, and the same pattern was reprinted prior to depositing the semiconductor. The other two, C and E, used the 25 nm alumina layer as a true buffer layer, where a single inhibitor printing was used sequentially to pattern the growth of the $Al_2O_3$ and the ZnO:N. Thus, the top surface of the buffer layer (C and E) was exposed only to the room atmosphere while gas flows were readjusted for ZnO:N. The ZnO:N thickness was 20 nm, and the AZO source and drain electrodes were patterned and deposited identically on all samples. A total of 134 devices were electrically tested on each substrate.

The yield and mobility results for this experiment are shown in the bar graph in Figure 5, with the wider bars corresponding

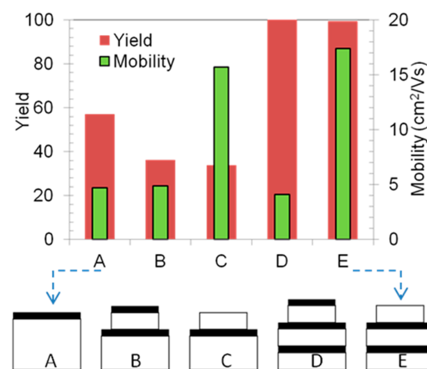


**Figure 5.** Yield and mobility of patterned-by-printing TFTs, with a cartoon illustration of the associated primary dielectric and buffer layer thickness and plasma treatment below. The thick black line corresponds to plasma treatment at that interface. Sample A had a 75 nm thick single-layer primary dielectric, plasma treated before ZnO:N; B had a 50 nm primary dielectric, with an added 25 nm $Al_2O_3$ layer that was plasma treated before ZnO:N; C was like B but with an $Al_2O_3$ buffer layer (no plasma-treatment); D had a two-layer primary dielectric with an added 25 nm $Al_2O_3$ layer that was plasma treated before ZnO:N; E was like D but with an $Al_2O_3$ buffer layer. Good yield is seen for multilayer dielectrics, plus higher mobility for devices with a buffer layer before ZnO:N.

to yield (deep orange, left-hand vertical axis), and the narrower bars corresponding to average mobility (green, right-hand vertical axis). In comparing the yields in this graph to those shown in Figure 2, it should be noted that the printed devices are many times larger than the photolithographic ones, and thus are expected to encounter more defects for a given defect density. The control substrate, A, had the thickest primary dielectric and a yield of nearly 60%. Both B and C, with a 50 nm thick primary dielectric, had yields below 40%. This corresponds to a defect density on the order of 100 shorting defects/$cm^2$, equivalent to the density we found for the much smaller-area lithographically processed devices with comparable dielectric. For the substrates with two-layer primary $Al_2O_3$, D and E, the yields were 99% and 100%, respectively. Thus, the control substrate with a single 75 nm dielectric layer had a better yield than the substrates with the single-layer 50 nm primary dielectric, as expected, but far worse than the substrates with a two-layer 50 nm primary dielectric.

As seen for substrates A, B, and D, the mobility of printed devices with the top dielectric surface exposed to an oxygen plasma before ZnO:N deposition was low, about 4.5 $cm^2/(V\ s)$, independent of the pattern of the layer. Conversely, when using a buffer layer the average mobility was about four times higher, at 16 and 17 $cm^2/(V\ s)$, respectively, as seen for substrates C and E.

Devices do not need to be designed with the source/drain pads wider than the semiconductor.[17] If the semiconductor area extends beyond the source and drain electrodes in the channel so that the approximate channel dimensions are determined by the source/drain geometry, then the entire area that the source/drain electrodes overlap with the gate is separated from the gate by the primary dielectric thickness, the buffer thickness, and also the ZnO:N thickness. This means thinner total dielectric can be used, with the benefit of lower voltage operation, because of the defect-reducing effects of the

additional layers. We have designed and fabricated patterned-by-printing devices, using both a two-layer dielectric and a buffer layer below the semiconductor, with individual TFTs, inverters, and ring oscillators (>90% overall yield). An example layout and output trace for a five-stage enhancement-mode ring oscillator, with an as-designed $\beta$-ratio of 2.67, is shown in Figure 6. The TFTs each had a 50 nm total gate dielectric,

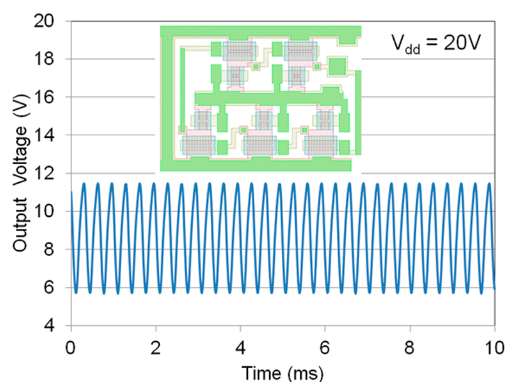


**Figure 6.** Five-stage ring oscillator performance at 20 V input voltage, with layout schematic inset. As-designed $\beta$-ratio was 2.67, the gate dielectric thickness was 50 nm, and the stage delay at this voltage was about 75 $\mu$s.

formed from two 15 nm $Al_2O_3$ primary dielectric layers, and a 20 nm buffer layer. The frequency is 2.68 kHz at an input voltage of 20 V. We have also fabricated substrates with more complex circuits.[18]

Because the "masks" consist of printed inhibitor ink, there is no time lag between layout and fabrication, allowing design cycles (design, fabrication, measurement, feedback) as short as 1 day or less. Our current print technology is useful to vet designs, materials, and processes. However, the ultimate speed of circuits fabricated with this printing process will always be limited. In our current practice, the minimum channel length is defined by the spread of a drop of inhibitor, and is between 70 and 90 $\mu$m. Furthermore, the circuits suffer from significant parasitic capacitance from source/drain overlap with the gate that is largely due to our low print resolution. However, the techniques developed with our current process are applicable to any scheme using printed inhibitor, including higher resolution printing methods.

## CONCLUSION

In summary, by designing interfaces carefully for the materials involved, we have demonstrated a robust process for printing electronics with high quality, good performance, and good yield in less than clean-room conditions. We can reliably and rapidly fabricate circuits by the combination of SAD and SALD, using a single insulating material, $Al_2O_3$, grown in steps separated by oxygen plasma treatment for improved yield, and using an $Al_2O_3$ buffer to protect the insulator/semiconductor interface for improved mobility.

## AUTHOR INFORMATION


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### Notes

The authors declare no competing financial interest.

## ACKNOWLEDGMENTS


The authors thank Andrew Thompson and Janet Barilla for technical assistance, Patrick Thompson for SIMS, Kenny Baptiste for AFM, and Manju Rajeswaren for XRD.


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